PREPARED BY: DATE	**SHARP**	SPEC NO. 'L A---o 51o3c
		FILE No.
APPROVED BY: DATE		ISSUE seD. 21.1994
	LIQU D CRYSTAL DISPLAY GROUP	PAGE *19*
	SHARP CORPORATION	APPLICABLE DIVISION '
		☐ DUTY DEVELOPMENT CENTER
	SPEC1F1CATION	☐ TFT DEVELOPMENT CENTER
		☐ LCD PRODUCTS DEVELOPMENT CENTER
		■ EL PRODUCTION DEPT.

SPECIFICATION FOR

EL Display Unit

MODEL No.   L J 6 4 H 0 3 4

☐ CUSTOMER'S APPROVAL

DATE _____

BY _____

PRESENTED

BY _~~signature~~_

H. Kishishita
Department General Manager
EL Production Department
Nara Factory
Liquid Crystal Display Group
SHARPCORPURATION

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RECORDS OF REVISION

	MODEL No. LJ64H034
	DOC. FIRST ISSUE
	1 DENT. DATA No.

DATE	REF. PAGE PARAGRAPH DRAWING No.	REVISED m	SUMMARY	CHECK & APPROVAL
May. 12.'93	Page 14	⚠	The content of a item 4 changed	7. Ohba
Feb. 9.'94	Page 2,4	⚠2	Elimination of former units.	H. Kokubota
	Page 1,4,12	⚠3	According as the revised LCD group standards.	
	Page 8	⚠4	Add Note 1) to item 7-3	
Sep. 21.'94	Page 7,8	⚠5	Addition of input signals timing characteristics.	H. Kokubota

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1. Application

This data sheet is to introduce the specification of EL display unit, LJ64H034.

2. Overview

The Sharp EL display unit consists of a thin film EL panel, high voltage ICs for panel driving and a display control circuit. By supplying eleven input signals of CMOS level and two DC power supplies of 15 V and 112 V arbitrary graphs and characters can be displayed.

3. Mechanical Specifications ⚠

Parameter		Specification				Unit
		Width x Height x Depth				
Outline dimensions	(Main unit)	246	x	175	x 18.0 (20.0*)	mm
	(DC-DC conv.)	158	x	30	x 17.0	
Number of matrix electrodes		640	x	400		--
Active area		I 191.9	x	119.9		mm
Dot pitch		0.3	x	0.3		mm
Dot pitch ratio		1	x	1		mm
Dot size		0.22	x	0.22		mm
Weight	(Main unit)	500 (540*)				g
	(DC-DC conv.)	40				

.Note)* With mounted DC-DC converter board.

Details of outline dimensions are shown at Page 12.

4. Absolute Maximum Ratings

4–1 Electrical absolute maximum ratings

$(Ta = 25\ ℃)$

Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	$V_L + 0.3$	V
Interface signal (Logic "L")	V_{IL}	-0.3	V
Supply voltage (Logic)	V_L	+7	V
Supply voltage (panel drive)	V_D	+14	V

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4 − 2 Environmental conditions ⚠

Parameter	Tstg		Topr		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature	-40 ℃	+80 ℃	-5 ℃	+55 ℃	Note 1)
Humidity	Note 2)		Note 2)		No condensation
Vibration	Note 3)		——		No operating
Shock	Note 4)		——		No operating

Note 1) Survival : -20℃ to +65℃

No permanent damage will occur.

Note 2) Ta≦40 ℃ ········· 95 %RH Max

Ta>40 ℃ ········· Absolute humidity shall be less than

Ta＝40 ℃／95 % RH.

Note 3) 5 ~ 55 Hz Frequency range

Sweep time ; 15 min each axis

Dwell at resonance; 10 min each resonance

Peak-to-peak

amplitude; 3.17 mm over 5 ~ 10 Hz range

1.52 mm over 10 ~ 25 Hz range

0.38 mm over 25 ~ 55 Hz range

55 ~ 500 Hz Frequency range

Sweep time ; 120 min each axis

Dwell at resonance; 30 min each resonance

Peak-to-peak

amplitude; 30 m/s² peak acceleration

Note 4) Acceleration ; 491 m/s²

Pulse width ; 11 ms

3 times for each direction of ±X/±Y/±Z.

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5. Electrical Characteristics

(Ta=25 ℃, Frame frequency= 120 Hz)

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Supply voltage (Logic)	V_L	+ 4.75	+ 5.0	+ 5.25	" v
Supply current (Logic, V_L=+5 V)	I_L	30	—	300	mA
Supply voltage (Panel drive)	V_D	+ 11.4	+12.0	+12.6	V
Supply current (Panel drive, V_D=+12 V	I_D	(※1)	—	1300	mA
Total power (V_L=+5 V, V_D=+12 V)	P_T	—	11	–	W

(※1) 10 mA in condition with no signals nor V_L supplying.

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6. Opical Characteristics ⚠ ⚠

(Ta=25 ℃, Frame frequency= 120 Hz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Luminance	L_{ON}	All dots lit	137	200	-	cd/m²	Note)
OFF luminance	L_{OFF}	All dots turned off	-	"	3.4	cd/m²	
Luminance distribution	ΔL_{DIS}	All dots lit	–	–	35	%	
Fill factor			Γ	0.54	·		Note 2)
Shadowing characteristics	ΔL_{SD}	fixed pattern	–	10	"	%	Note 3)
Viewing angle			·	160	–	°	

Note1) Average luminance measured at the five circular windows (R1~R5)

shown in Fig. 1 (Circular window diameter: ϕ 13 mm)
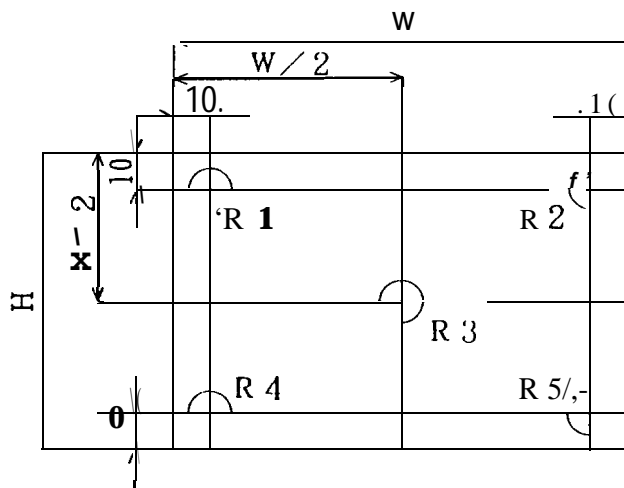
Fig. 1

H 119.9   : Height of active area

W 191.9   : Width of active area

Un t   : mm

To erance of
      luminance: ± 10 %

The following formula defines the luminance distributio

$$\Delta L_{DIS} = (\quad - \frac{L_{MIN}}{L_{MAX}}) \times 100 \, (\%)$$

where L_{MAX} is the max mum luminance and L_{MIN} is the min mum uminance taken
at the five locations in Fig. 1.

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Note 2)   The ratio of the emission area to the d splay area. •••••• SHARP's EL
has comparatively high fill factor, and therefore, the visibility
of display is excellent.

Note 3) Shadow ng characteristics means the variation of luminance accord-
ing to the number of dots lit on a scanning line.

Thanks to the addition of the shadowing compensation circuit, the
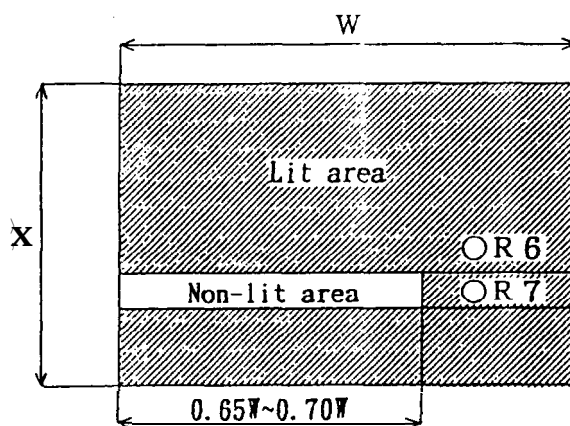display quality of SHARP's EL is improved.

Fig. 2

The following formula defines the shadowing characteristics:

$$\Delta L_{SD} = (\frac{L_N}{L_L} - 1) \times 100 \ (\%)$$

where L_L is the luminance at R_6. L_N at R_7.

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7. Timing Characteristics

7 − 1 Input signals

This unit is driven by line-at-a-time scanning method with following 11 CMOS level input signals.

Parameter	Symbol	Description	
Data input clock signal	C P 2	Clock signal for inputting the display data into the EL unit.	
Display data signal	U D 0~3	Data signal for the upper part of display	The signals are sampled at every falling edge of the data input clock signal. The display is 'ON" while the logic is "H" and "OFF" while the logic is "L".
	L D 0~3	Data signal for the lower part of display	
Input data latch signal	C P 1	This signal controls the "timing of line-at-a-time scanning" and the "latch timing of the data side shift register on falling edge." '	
Scan start-up signal	S	This signal controls frame frequency. And the contents of the display data signal are displayed on the first line by combination with this signal.	

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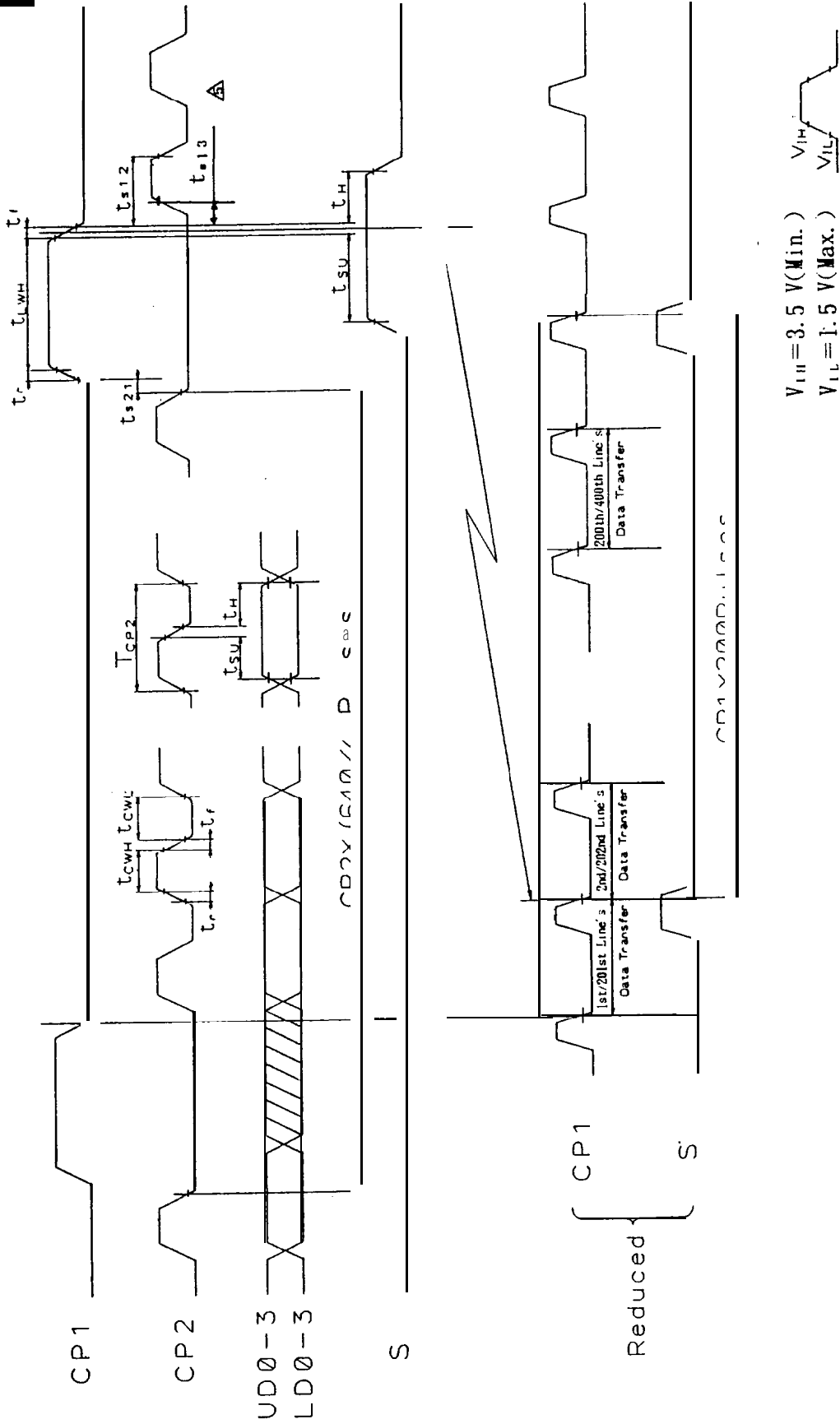
7-2 Input signals timing characteristics

(Ta=25 ℃)

Parameter	Symbol	Min.	Typ.	Max.	unit
Frame frequency	$1/T_{FRM}$	60	-	120	H z
CP2 clock cycle	T_{CP2}	182	—	—	n s
High level clock width	t_{CWH}	60	-	—	n s
Low level clock width	t_{CWL}	60	-	—	n s
CP1 clock cycle	t_{CP1}	40		—	μ s
High level latch clock width	t_{LWH}	60	-	—	n s
Data set up time	t_{SU}	50	—	—	n s
Data hold time	t_{H}	40	—	—	ns
CP1↑clock allowance time from CP2↓	t_{S21}	0	-	—	n s
CP2↓clock allowance time from CP1↓	t_{S12}	200	-	—	n s
CP2f clock allowance time from CP1↓	t_{S13}	100	-	—	n s
Clock rise/fall time	t_r, t_f	"	-	t_{rf} *	n s

A

* $t_{rf} = (T_{CP2} - t_{CWH} - t_{CWL}) / 2 S 3 0$ n s

Note) The vertical blanking time $(T_{FRM} - T_{CP1} \times 200)$ shal be minimized to avoid the flickering lines around the center of the d splay.(around 200th and 201th horizontal lines)
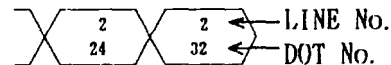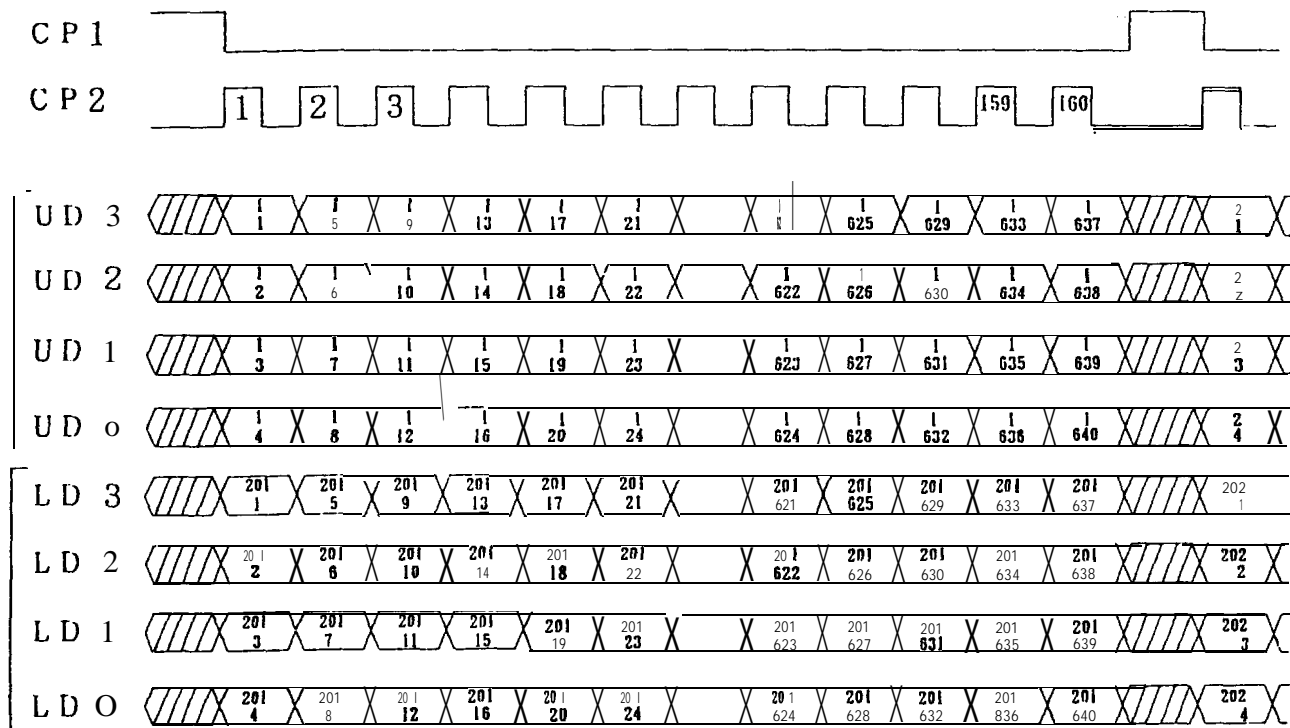
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7-3 Input signals timing chart.

CP1

CP2

UD0-3
LD0-3

S

Reduced { CP1
          S

t_r t_{WH} t' t_{s12} t_{s13}

t_{s21} t_H t_{SU}

t_{CWH} t_{CWL} t_f T_{CP2} t_H t_{SU}

1st/201st Line's Data Transfer   2nd/202nd Line's Data Transfer   200th/400th Line's Data Transfer

$V_{IH} = 3.5\,V(Min.)$
$V_{IL} = 1.5\,V(Max.)$

V_{IH}
V_{IL}

Note 1) CP1 × 200 pulses shall kept.

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7 − 4 Data transmission timing.

	2		2	← LINE No.
	24		32	← DOT No.

7 − 5 Transmission data and relative position on panel.

LINE ↓ / DOT →	1	2	3		639	640
1	1−1	1−2	1−3			
2	2−1	2−2	2−3			
3	3−1	3−2	3−3			
uD ⋮						
199	199−1	199−2	199−3		199−639	199−640
200	200−1	200−2	200−3		200−639	200−640
201	201−1	201−2	201−3		201−639	201−640
202	202−1	202−2	202−3		202−639	202−640
203					203−639	203−640
LD ⋮						
399	399−1	399−2	399−3		399−639	399−640
400	400−1	400−2	400−3		400−639	400−640

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8. Interface signals and power supply connectors

Assignment of pins of connector CN5

No.	SIGNAL	No.	SIGNAL
1	UD1	2	UDO
3	UD3	4	UD2
5	LD1	6	LDO
7	LD3	8	LD2
9	CP2	10	GND
11	CP1	12	GND
13	s	14	GND
15	GND	16	GND
17	+ 5 V	18	+ 5 V
19	+12 V	20	+12 V

Arrangement of pins of connector CN5

```
 1   3   5   7   9    11 13  15  17  19
 □   □  c1   □   □   □   □   □   □  •1


 □   □   □   □   □   □   □   ❏   □   □
 2   4   6   8     10  12  14  16  18  20
```
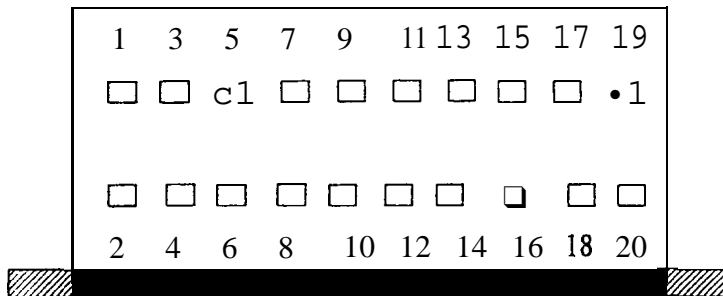
(Fig. 3)

Connectors

	Model No.	Maker
Unit-side pin header	DF11-20DP-2DS or equivalents	HIROSE ELECTRIC CO.
Fitting socket (crimp contact)	DF11-20DS-2C or equivalents (DF11-2428SC)	HISOSE ELECTRIC CO.

Note 1) The length of the cable shall not exceed 50 cm.

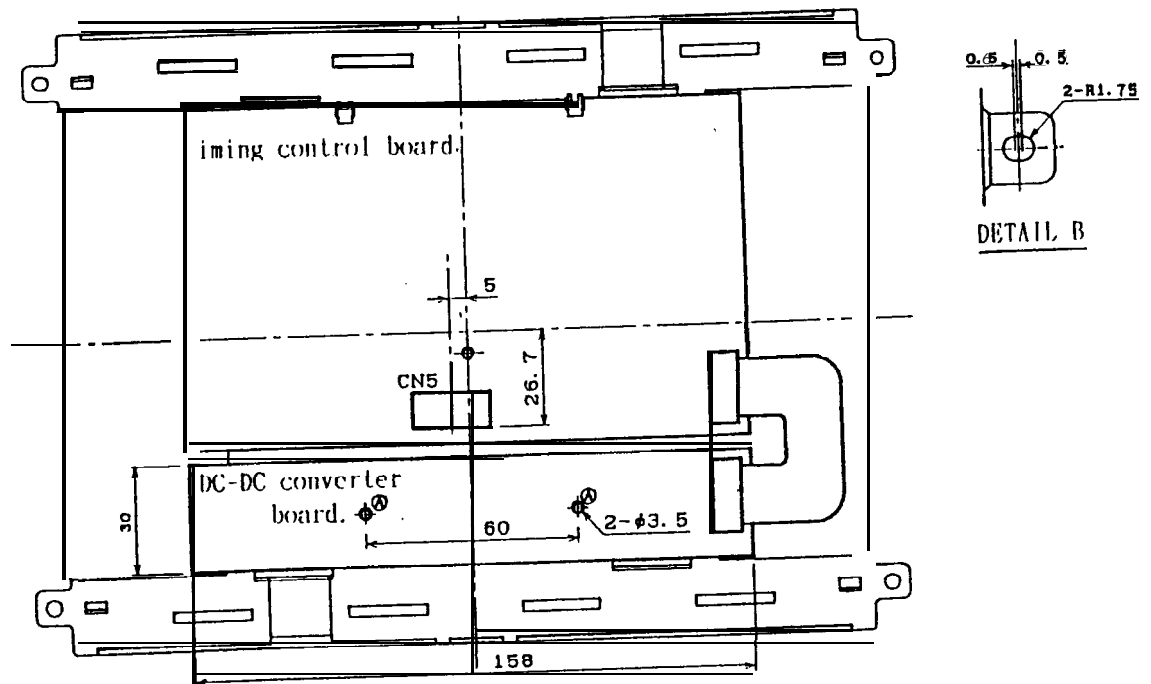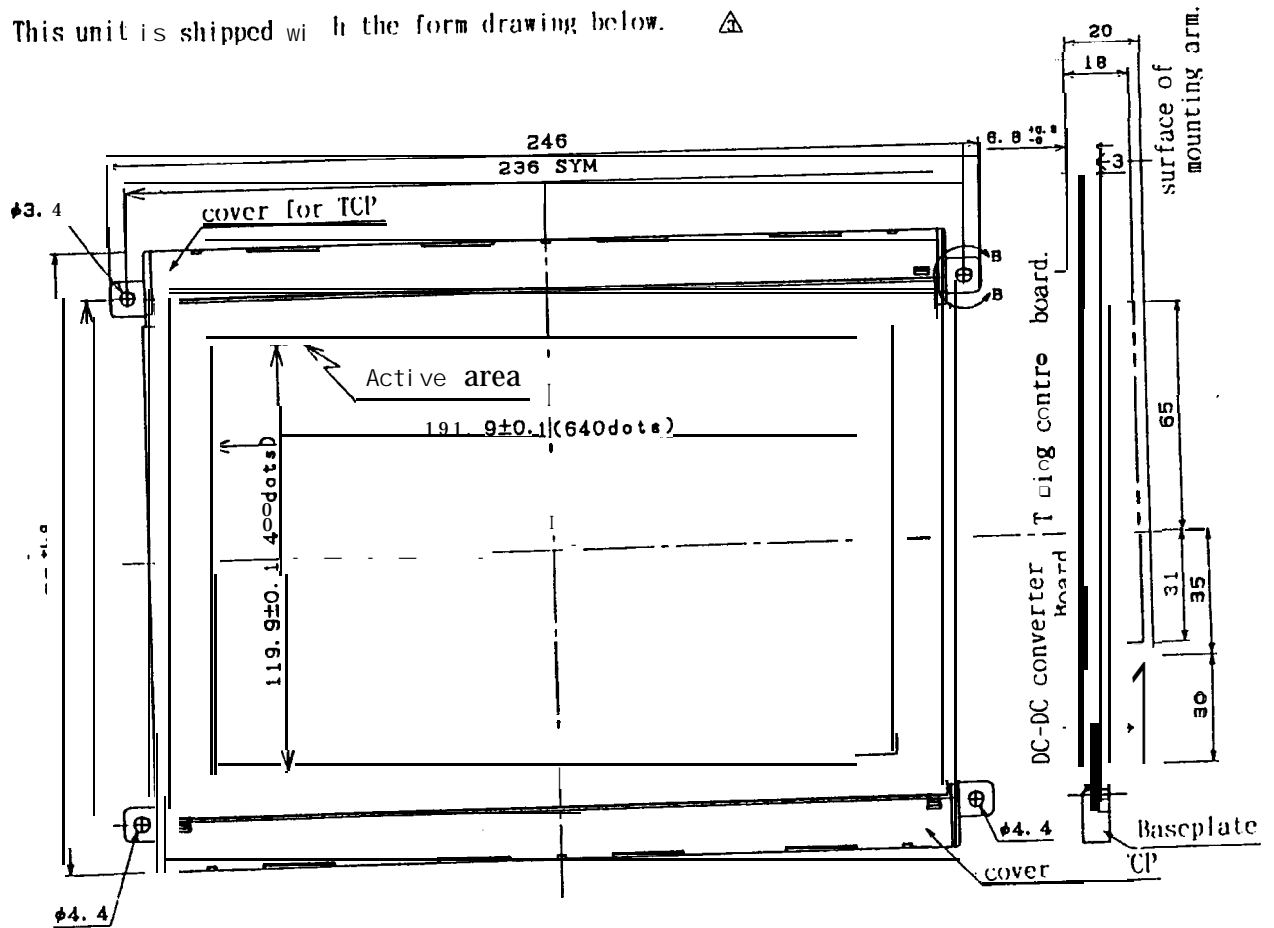Note 2) This unit is not supplied with the fitting socket and the cable.

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9. Functional Block Diagram

Column Electrode Driver ICs

EL Panel
640×400 lines

Row Electrode Driver ICs

Column Electrode Driver ICs

-f,

Write Driver Circuit 2

Write Driver Circuit 1

Modulation Drive Circuit

Oscilllator/ Diivider Ciircuit

Voltage Doubler Circuit

DC-DC Comverter Ciircuit

Timing Control Circuit

C P 2

UD0~3

LD0~3

C P 1

S

GND

+5 V

+12 V

11 input signals   power supply
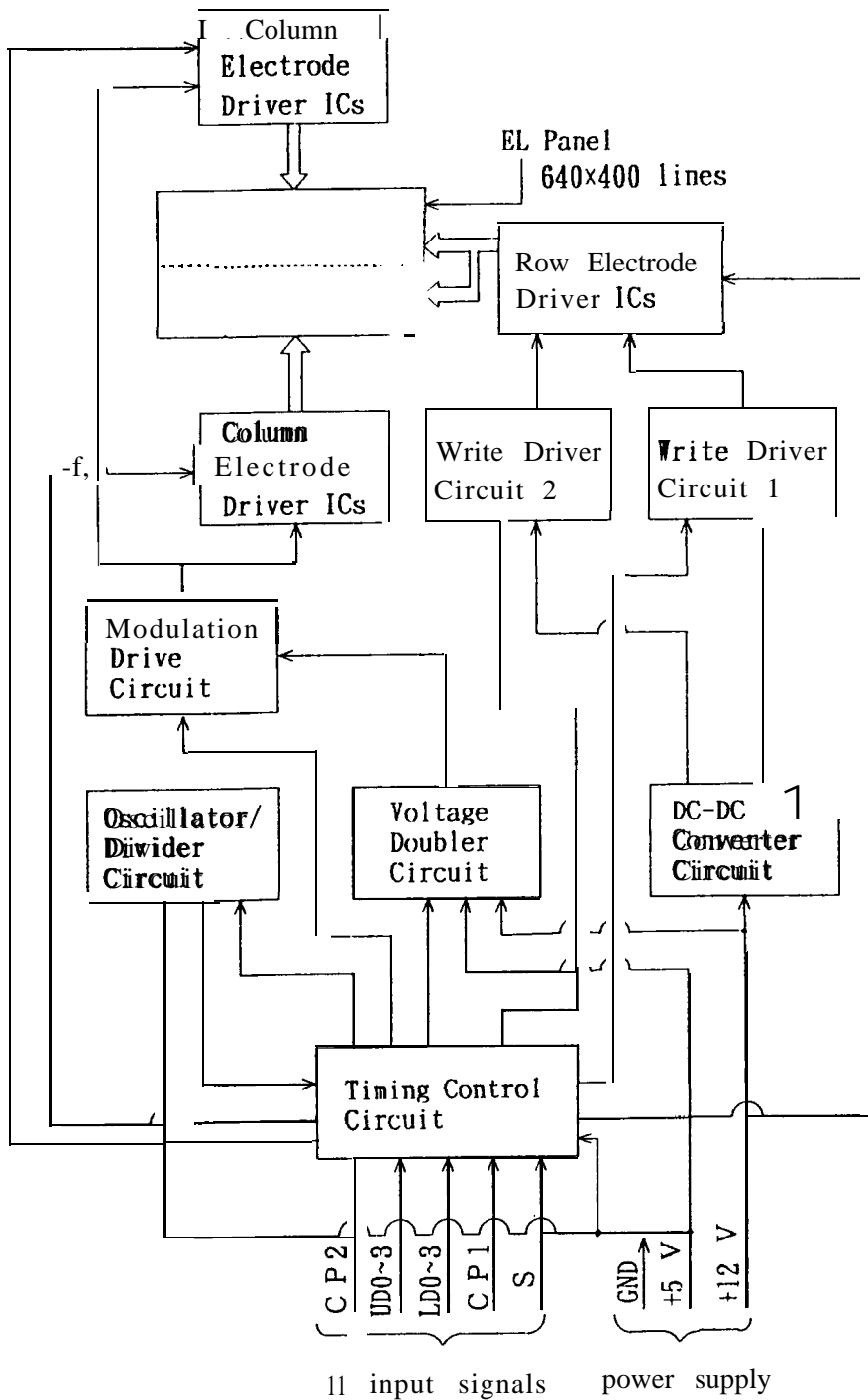
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10. Outline of the unit configuration

This unit is shipped with the form drawing below. ⚠

Active area

191.9±0.1 (640 dots)

cover for TCP

246

236 SYM

6.8

DC-DC converter board.

Timing control board.

surface of mounting arm.

20

18

65

31

35

30

φ3.4

φ4.4

φ4.4

Baseplate

cover

DETAIL B

2-R1.75

0.65   0.5

iming control board.

CN5

DC-DC converter board.

5

26.7

30

60

2-φ3.5

158

Note) Unspecified tolerance to be ±0.5.

(Unit: mm)

(Fig. 4)

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The DC/DC converter board of the EL unit is detachable for lower profile
(20->18 mm). The detachment can be made with the screws (A) in the Fig. 4
in Page 12.

〈Precautions for detaching DC/DC converter board〉
1. The unit shall not be operated during the procedure with due care for ESD.
2. The DC/DC converter board is hazardous with its output +250 VDC and -200 VDC. Handle with care when the board is installed into host system.
3. The cable shown in Fig. 6 is attached between the main controller board and DC/DC converter board. If an extension is required, the total length of the extended cable shall be not longer than 200 mm and the cable shown in the Table. 1 or equivalent one shall be prepared.
4. The output voltage of the DC/DC converter board is factory preset for the optimum value to match the individual panel characteristics.
   Make sure the coupling of the DC/DC converter board and its host EL unit shall be mainlined.

Timing control board.

5

CN5   26.7   CN 6

t

DC-DC converter board.   60   2-φ3.5   CN7

C N 7 P W B

MAX 12   MAX 3
MAX 17

(DC-DC converter board side view)

(Fig. 5)

ℓ = 60 mm

6   6
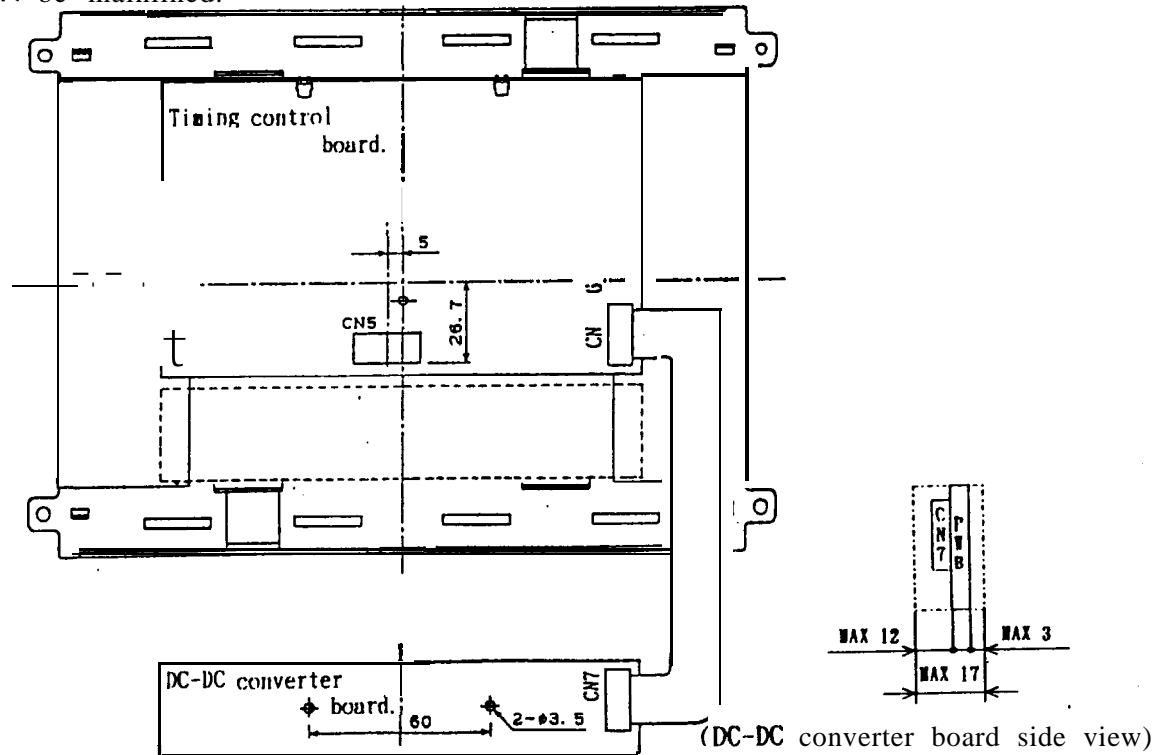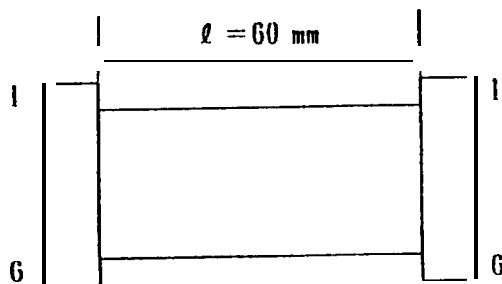
(Fig. 6)

	Model No.	Maker
CN6, 7	DF1B-6P-2.5DS	HIROSE
Cable-side connector		
● sockeL	DF1B-6S-2.5R	"
● crimp contact	DF1B-2428SC	"
● wire	AWG#24, 300 V/80 ℃	—

(Table. 1)

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11. Handling Instructions and Cautions for Operation

<u>Handling   Instructions</u>

1. Handle the unit with care of ESD, The operator and the place around him
   must be guard against ESD.
   Hold the mounting arms of 4 corners of the uni   when you handle it.

2. Since the EL panel is made of glass, care shal   be taken to avoid the
   breakage caused by dropping or bumping it.

3. The display control board or the cover for TCP shall not be removed
   nor the unit shall be disassembled. ICs mounted on the unit shall never
   be touched by fingers/hands to prevent the breakage due to static
   electricity.

4. Please use the packaging form shown on page 18 at any shipment. There is
   a high possibility for the unit to be broken without using packaging.
   carton used at our shipment to you.
   on using other packaging form than the one shown on page 18 at any
   shipment, please be careful to prevent glass and PWB from being under
   Pressure, using shock absorber.


<u>Cautions for operation</u>

1. The unit shall be operated within the rated operating cond t ons
   specified in this literature.
   When you mount the unit on your product, design your product making the
   unit breathable.

2. operation of the unit at high temperature with high humidity shall be
   strictly avoided.
   Dew on the connector or on the circuits will cause malfunction, which can lead d
   amage to the unit.

3. The display control board on the rear side of the unit shall never be
   touched while in operation. It generates AC pulse of approx. 200 V.

⚠ 4. To avoid the image retention caused by the luminance change due to time
   lapse, and to increase the panel life, please pay attention to the design
   of display, so that a fixed pattern may not be displayed as possible as
   you can, and by using all parts of the viewing area evenly.
   Also, we would recommend to use the unit at the ambient temperature as
   low as you can because the temperature is one of the causes of acceleration
   of the luminance change due to time lapse.

<u>Others</u>

If any problem should arise from this specification, the supplier and user
should work out a mutually acceptable solution.

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12. Circuit scheme of the s gnal input block

UD0

UD1

UD2

UD3

LD0

LD1

LD2

LD3

CP2

CP1

S

IC1
LZ95N37
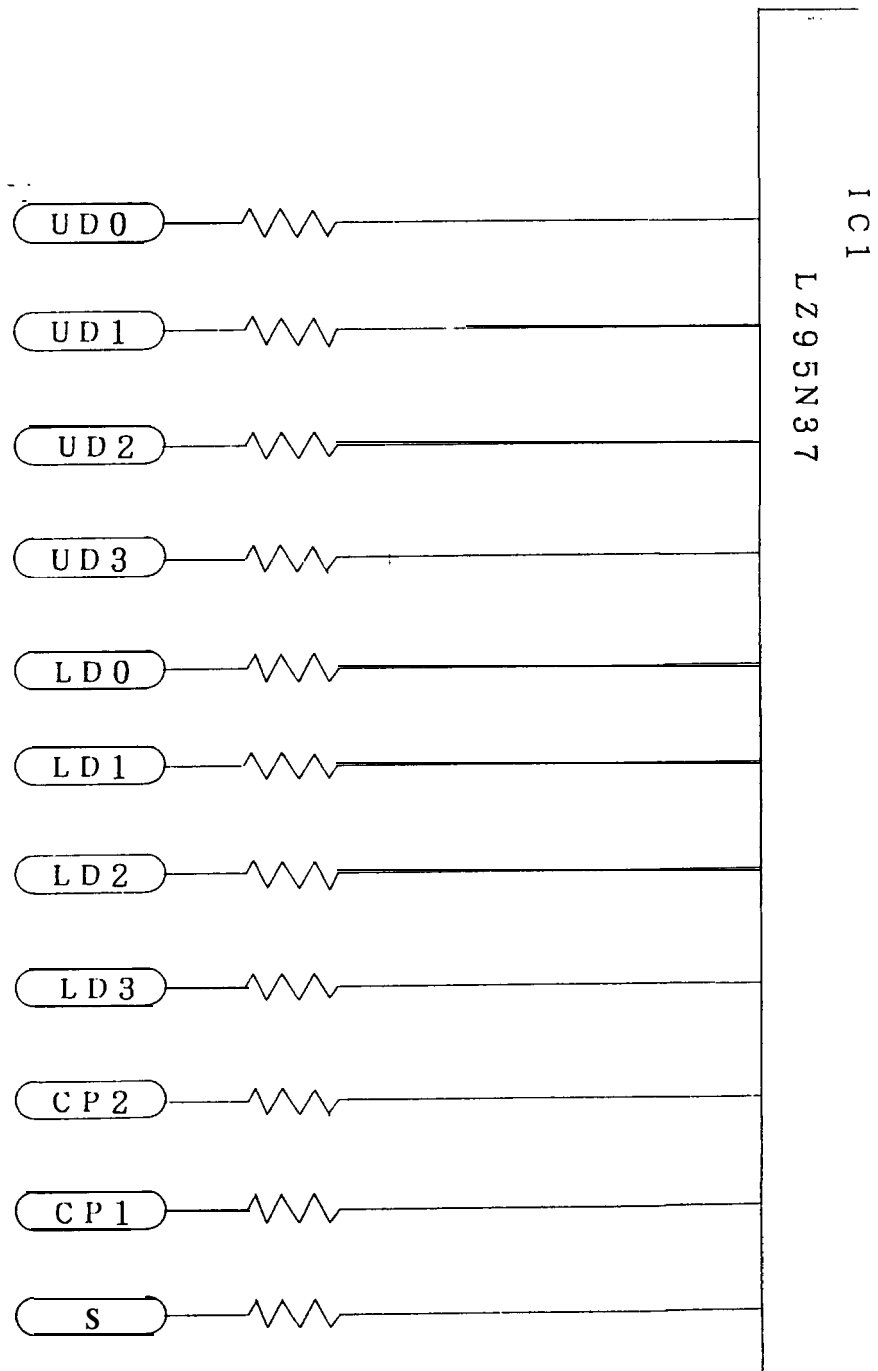
47Ω × 11

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13. Power supply input circuit

(a) Over current protection

This unit equips fuses in power supply input circuit protecting fire accident rising from over current in internal circuit, so the fuse may melt down when the specifications are not kept or in case of short circuit.
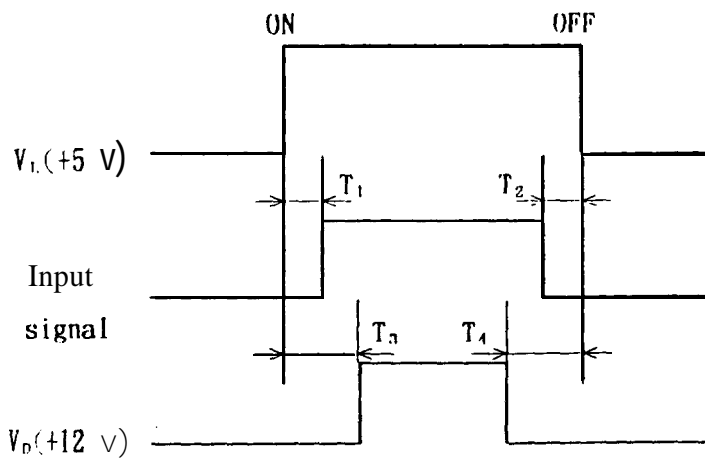
Fuse specifications

Parts No.	Model No.	Ratings	Melt type	Anthorizaition Standard
F 1	SSFR630mAF003 ✻	630 mA	quick melt down	UL. CSA
F 2	SSFR1. 6AF003 ✻	1.6A	"	"
F 3	SSFR1. 6AF003 ✻	1.6A	"	"

✻: or equivalents   Maker : S. O. C.

Note) Fuses is not open in the case current capacity of power supply is small. [In the other hand fuses is open by surge current in case of current capacity of power supply is big or supply power to the unit using relays. In consequence please you thoroughly investigate the unit.
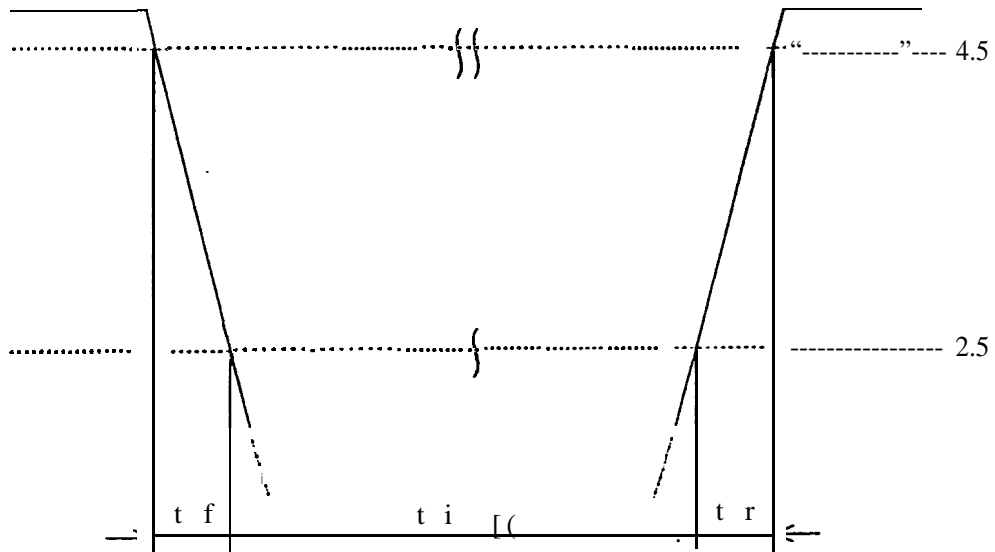
(b) Power on/off sequence

Note) $T_{1\sim4} \geq 0$ shall be kept.

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(c) Take account of the sheme below for 5 VDC input
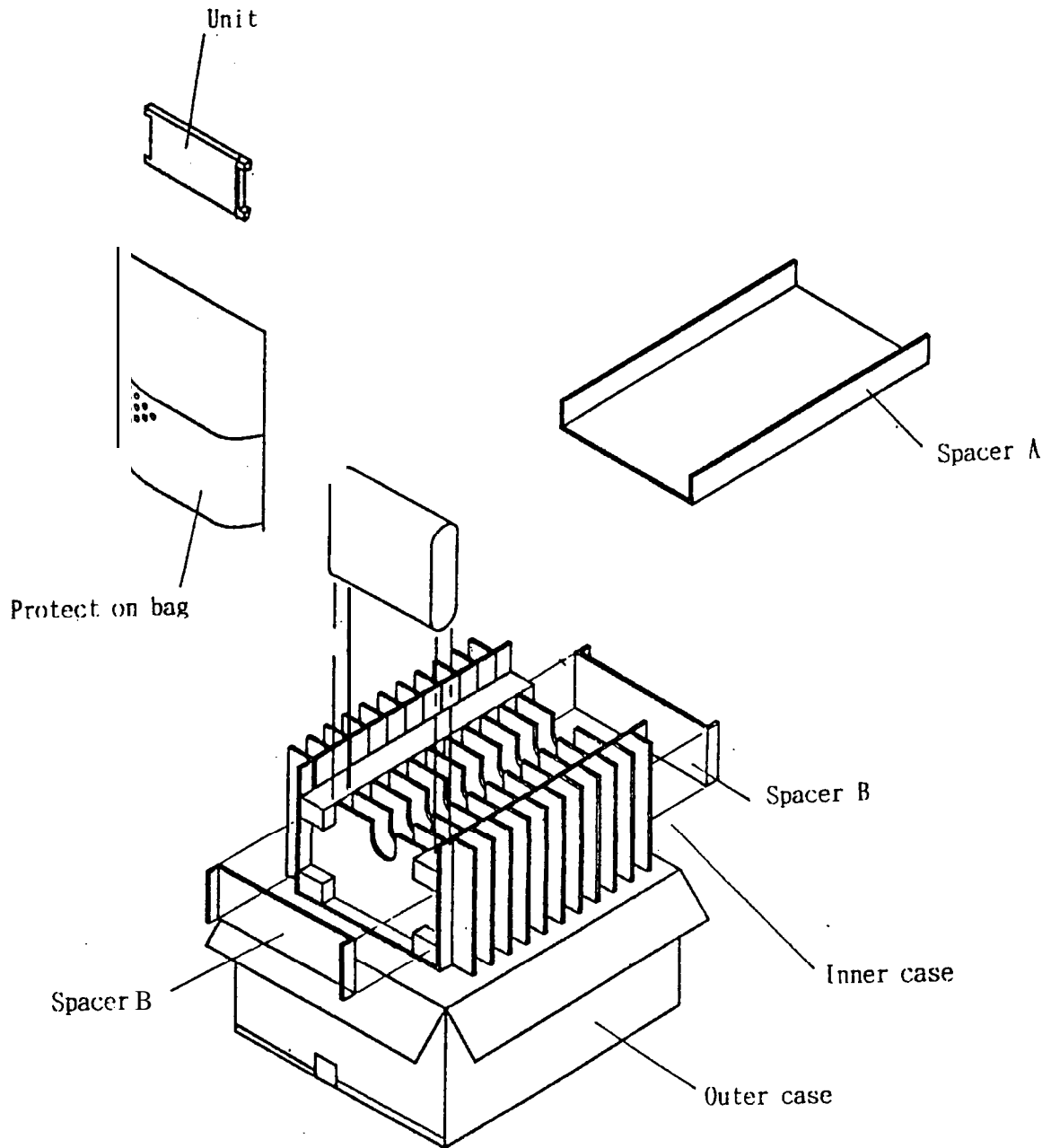   rising up time and falling down time of 5 VDC

tf = fall ng down time   tr = rising up **time**

(1) tf, tr $\leqq$ 100 ms is better to be kept.

(2)   ti $\geqq$ 1 ms shall be kept.

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14. Packing   specification

10pcs./package

Unit

Spacer A

Protect on bag

Spacer B

Inner case

Spacer B

Outer case

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Outline

335

615

385